IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1-6 (Canceled)

7. (Currently amended) A method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising the steps of:

forming a device isolation film in a given region on a semiconductor substrate to define an active region and a device isolation region;

defining said active region into a cell region and a peripheral circuit region by a given process;

forming a tunnel oxide film and a first polysilicon film on the entire structure including the device isolation film and then patterning said tunnel oxide film and said first polysilicon film so that said tunnel oxide film and said first polysilicon film remain in a given region of said cell region, thus defining a floating gate;

sequentially forming an insulating film ~~including an oxide film and a nitride film~~ and a second polysilicon film on the entire structure including said cell region and said peripheral circuit region, the insulating film including an oxide film and a nitride film and being formed under the second polysilicon film;

patterning said second polysilicon film and said insulating film so that they can remain only in a given region of said cell region and said peripheral circuit region, respectively, thus forming a control gate of the flash memory cell on the insulating film covering the floating gate in said cell region respectively, and a gate of the code address memory cell on the insulating film covering a surface of the substrate in said peripheral circuit region; and

performing an impurity ion implantation process for a given region of said semiconductor substrate to form a source region and a drain region, so that a flash memory cell including the tunnel oxide film, the first polysilicon film, the insulating film and the second polysilicon film is formed in said cell region, and a code address memory cell including the insulating film and the second polysilicon film is formed in said peripheral circuit region.

8. (Previously Presented) The method manufacturing a code address memory cell according to claim 7, wherein said insulating film is formed by stacking at least two or more layers of at least one of said oxide film and said insulating film.

9. (Previously Presented) The method manufacturing a code address memory cell according to claim 7, wherein said insulating film has a thickness of about 30~300□.

10. (Previously Presented) The method manufacturing a code address memory cell according to claim 7, wherein said insulating film is formed by stacking a first oxide film, a nitride film and a second oxide film.

11. (Previously Presented) The method manufacturing a code address memory cell according to claim 7, wherein said insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film and a second nitride film.

12. (Previously Presented) The method manufacturing a code address memory cell according to claim 7, wherein said insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film, a second nitride film and a third oxide film.

13. (Currently amended) A method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising the steps of:

forming a device isolation film in a given region on a semiconductor substrate to define an active region and a device isolation region;

defining said active region into a cell region and a peripheral circuit region by a given process;

forming a tunnel oxide film and a first polysilicon film on the entire structure including the device isolation film and then patterning said tunnel oxide film and said first polysilicon film so that said tunnel oxide film and said first polysilicon film only remains in a given region of said cell region, thus defining a floating gate;

sequentially forming an insulating film and a second polysilicon film on the entire structure including said cell region and said peripheral circuit region, wherein said insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film, a second nitride film and a third oxide film;

patterning said second polysilicon film and said insulating film so that they can remain only in a given region of said cell region and said peripheral circuit region, respectively, thus forming a control gate of the flash memory cell on the insulating film covering the floating gate in said cell region, and a gate of the code address memory cell on the insulating film covering a surface of the substrate in said peripheral circuit region; and

performing an impurity ion implantation process for a given region of said semiconductor substrate to form a source region and a drain region, so that a flash memory cell including the tunnel oxide film, the first polysilicon film, the insulating film and the second polysilicon film is formed in said cell region, and a code address memory cell including the insulating film and the second polysilicon film is formed in said peripheral circuit region.